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3. Write The Verilog Program For Your Design (e.g.: Codefile1.v) Gedit Codefile1.v 4. Write The Verilog Test Bench Program For Your Design (e.g.: Codefile1\_tb.v). Now, The Design Entry Using HDL Gets Finished. Gedit Codefile1\_tb.v II. STEPS FOR SIMULATION: 1. Initially, Both Of Your Verilog Programs Have To Be Compiled 2. Jan 1th, 2024

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3 Tunca Kortantamer; <sup>3</sup>Gl Kasidesi, Eski T Rk Edebiyatı Makaleler, Akçağ Yayınları, Ankara 1993. 4 Cem Dilcin; <sup>3</sup>Fuzuli'nin Bir Gazelinin ùerhi Ve Yapısal Yönden İncelenmesi, Trkoloji Dergisi, Cilt 9, 1991, S. 43-98. 5 Dursun Ali Tökel, <sup>3</sup>Ontolojik Analiz Metodu Ve Bu Metodun Baki'nin Apr 1th, 2024

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Group Theory Representation Of Groups: Preparation Of Matrices And Vectors, Matrix Notations For Geometrical Transformations, Orthogonality Theorem And Its Consequences, Reducible And Irreducible Representations And Their Relation, Preparation Of Character Table For C2v,D2h, Mar 1th, 2024

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