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Lecture 14 Field Effect Transistor (FET)

Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) JUNCTION FIELD EFFECT TRANSISTOR (JFET) FET 1-5 . Construction Of JFET FET 1-6 . Characteristics Of JFET By Applying Voltage At The JFET's Terminal ($V_{GS} = 0 \text{ V}$ And $V_{DS} = +ve \text{ Values}$), Some Characteristics Can Be Obtained For The N-type Material, Electrons Will Be Attracted To The Positive Terminal Of V_{DS} For The P-type Material At ... 1th, 2024

PMV213SN UTrenchMOS(tm) Standard Level FET

P_{der} 03aa25 0 40 80 120 0 50 100 150 200 T_{sp} ($^{\circ}\text{C}$)
 I_{der} (%) P_{der} P_{tot} P ... Package Outline Fig 14. SOT23.
UNIT A1 Max. B P_{cDE} E1 HE L Qwv OUTLINE
REFERENCES VERSION EUROPEAN PROJECTION ISSUE
DATE 97-02-28 99-09-13 IEC JEDEC EIAJ Mm 0.1 0.48
0.38 0.15 0.09 3.0 2.8 1.4 1.2 2th, 2024

Si9410DY N-channel TrenchMOS™ Logic Level FET

Pder (%) 03aa19 0 40 80 120 0 50 100 150 200 (C)
Ider (%) Pder Ptot P ... Package Outline Fig 14.
SOT96-1 (SO8). UNIT A Max. A1 A2 A3 Bp CD (1) E(2)
EH (1) E LLp QZv W Y ... 3th, 2024

PHD16N03LT N-channel TrenchMOS™ Logic Level FET

Pder (%) 03aa24 0 40 80 120 0 50 100 150 200 Tmb
°C) Ider (%) Pder Ptot P ... Plastic Single-ended Surface
Mounted Package (Philips Version Of D-PAK); 3 Leads
(one Lead Cropped) SOT428 E B2 E1 B1 BcwAM L L1
13 2 D D1 HE L2 Note 1. Measured From Heatsink Back
To Lead. E1 E A A2 A A Y Seating Plane Mounting 1th,
2024

PMGD280UN Dual N-channel μTrenchMOS Ultra Low Level FET

7. Package Outline Fig 14. SOT363 (SC-88). OUTLINE
REFERENCES VERSION EUROPEAN PROJECTION ISSUE
DATE IEC JEDEC EIAJ SOT363 SC-88 Bp WBM D E1 E Pin
1 Index A A1 Lp Q Detail X HE E V M A B A Y 0 1 2 Mm
Scale C X 132 6 5 4 Plastic Surface Mounted Package;
6 Leads SOT363 UNIT A1 Max Bp CDE E1 HE Lp Qyv W
Mm 0.1 0.30 0.20 2.2 1.8 0.25 0.10 1.35 1.15 ... 1th,
2024

BUK71/7907-55AIE TrenchPLUS Standard Level

FET

Pder (%) 03ni63 0 40 80 120 160 0 50 100 150 200
Capped At 75A Due To Package Tmb (°C) ID (A) Pder
Ptot P Tot 25 C()° = -----×100% 03nf55 1 10 102 103 1
10 102 VDS (V) ID (A) DC 100 Ms 10 Ms Limit RDSon =
VDS/ID 1 Ms Tp = 10 µs 100 µs Capped At 75 A Due To
Package 1th, 2024

PHP/PHD3055E TrenchMOS Standard Level FET

9. Package Outline Fig 15. SOT78 (TO-220AB).
OUTLINE REFERENCES VERSION EUROPEAN
PROJECTION ISSUE DATE IEC JEDEC EIAJ SOT78
SC-463-lead TO-220AB D D1 Q P L 12 3 L1(1) B1 E E B
0 5 10 Mm Scale Plastic Single-ended Package;
Heatsink Mounted; 1 Mounting Hole; 3-lead TO-220AB
SOT78 DIMENSIONS (mm Are The Original Dimensions)
E A A1 C Note 1 ... 2th, 2024

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