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•21 11/1/2006 VLSI Design I; A. Milenkovic 41 Min-Delay: Pulsed Latches Tt T Tcd

Ccq Pw $\geq$ -+hold CL Q1 D2 Q1 D2  $\phi$  P T Pw  $\phi$  P L1  $\phi$  P L2 T Cd T Hold T Ccq Hold

Time Increased By Pulse Width 11/1/2006 VLSI Design I; A. Milenkovic 42 Time

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